CLAIMS

What is claimed is:

1. A method of assembling a flip-chip semiconductor device assembly, the method comprising:

providing a wafer having an active surface and a back surface and including a plurality of unsingulated semiconductor dice, at least some semiconductor dice of said plurality having conductive bumps protruding transversely from said active surface;

providing a wafer scale interposer substrate having a first surface and a second surface, said wafer scale interposer substrate including a plurality of unsingulated interposer substrates, each having conductive elements thereon adjacent said second surface, each unsingulated interposer substrate dimensioned and located to correspond with one of said plurality of semiconductor dice of said wafer, each of said plurality of interposer substrates having a plurality of recesses extending thereinto from said first surface to expose at least a portion of one of said conductive elements; and

placing said wafer with said active surface thereof facing said first surface of said wafer scale interposer substrate and said unsingulated semiconductor dice in alignment with said unsingulated interposer substrates and disposing each of said conductive bumps protruding transversely from said active surface into a recess of said plurality of recesses of said interposer substrates so that said conductive bumps are substantially received within said plurality of recesses in said interposer substrates.

2. The method of claim 1, further comprising attaching said active surface of said wafer directly to said first surface of said wafer scale interposer substrate by at least one adhesive element disposed on said first surface at a location of each of said plurality of interposer substrates.

3. The method of claim 1, wherein said disposing comprises abutting said active surface of said wafer with said first surface of said wafer scale interposer substrate.

4. The method of claim 1, further comprising aligning each of said conductive bumps on said at least some semiconductor dice with said plurality of recesses so that each of said conductive bumps is positioned directly over one of said plurality of recesses.

5. The method of claim 1, wherein said providing said wafer scale interposer substrate comprises forming said plurality of recesses to be sized and configured to substantially receive said conductive bumps therein.

6. The method of claim 1, wherein said providing said wafer scale interposer substrate comprises forming said plurality of recesses collectively in each of said semiconductor dice in at least one of a centrally aligned row configuration, a peripheral configuration and an I-shaped configuration.

7. The method of claim 1, wherein said disposing comprises positioning said conductive bumps of said semiconductor dice in said recesses of said plurality of an interposer substrate so that a surface of each of said conductive bumps directly contacts a conductive element.

8. The method of claim 1, further comprising bonding each of said conductive bumps to a said conductive element.

9. The method of claim 8, wherein said bonding comprises bonding by at least one of reflowing, curing, ultrasonic bonding and thermal compression bonding.

10. The method of claim 1, further comprising disposing a nonsolid conductive material on said conductive bumps prior to disposing said conductive bumps in said plurality of recesses.

11. The method of claim 10, further comprising bonding each of said conductive bumps having said nonsolid conductive material thereon to a said conductive element using said nonsolid material.

12. The method of claim 1, further comprising disposing a nonsolid conductive material in each of said plurality of recesses.

13. The method of claim 12, wherein said disposing said nonsolid conductive material comprises:

providing a stencil having a pattern of apertures therethrough corresponding to a pattern of said plurality of recesses of said unsingulated interposer substrates of said wafer scale interposer substrate;

positioning said stencil over said wafer scale interposer substrate so that said pattern of apertures corresponds with said pattern of said plurality of recesses; and

spreading said nonsolid conductive material over said stencil and into said plurality of recesses with a spread member.

14. The method of claim 12, further comprising inserting each of said conductive bumps in a recess of said plurality of recesses in contact with said nonsolid conductive material therein.

15. The method of claim 14, further comprising bonding each of said conductive bumps inserted in said recesses to said conductive elements using said nonsolid conductive material.

16. The method of claim 1, wherein said providing said wafer scale interposer substrate comprises providing said wafer scale interposer substrate with at least one opening in said first surface thereof at a location of each interposer substrate and placing and configuring said at least one opening to communicate with at least one recess of said plurality of recesses.

17. The method of claim 16, further comprising introducing dielectric filler material through said at least one opening into a space adjacent said conductive bumps in said at least one recess.

18. The method of claim 1, further comprising introducing dielectric filler material into a space adjacent at least some of said conductive bumps disposed in said plurality of recesses.

19. The method of claim 1, wherein said providing said wafer comprises providing a layer of encapsulation material on said back surface thereof

20. The method of claim 19, wherein said providing said layer of said encapsulation material is effected by at least one of spin-coating and glob-top covering.

21. The method of claim 18, further comprising dicing said wafer and said wafer scale interposer substrate into singulated semiconductor device assemblies, each of said singulated semiconductor device assemblies comprising at least one semiconductor die of said plurality of semiconductor dice secured to at least one interposer substrate of said plurality of interposer substrates.

22. The method of claim 21, further comprising at least partially encapsulating said singulated semiconductor device assemblies by dispensing encapsulation material about a periphery of said at least one semiconductor die of each of said singulated semiconductor device assemblies.

23. The method of claim 1, further comprising dicing said wafer disposed to said wafer scale interposer substrate into singulated semiconductor device assemblies, each of said singulated semiconductor assemblies comprising at least one semiconductor die of said plurality of semiconductor dice secured to at least one interposer substrate of said plurality of interposer substrates.

24. The method of claim 23, further comprising at least partially encapsulating said singulated semiconductor assemblies by dispensing encapsulation material about a periphery of said at least one semiconductor die of each of said singulated semiconductor device assemblies.

25. The method of claim 24, wherein said at least partially encapsulating said singulated semiconductor device assembles comprises leaving said back surface of said at least one semiconductor die exposed.